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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	:	Masato MORI et al.	Group Art Unit: 1793
Appln. No.	:	10/597,949 (U.S. National Stage of PCT/JP2005/003043)	Examiner: PATEL, DEVANG R
I.A. Filed	:	February 24, 2005	Confirmation No. : 8311
For	:	ELECTRONIC COMPONENT MOUNTING METHOD, AND CIRCUIT SUBSTRATE AND CIRCUIT SUBSTRATE UNIT USED IN THE METHOD	

RESPONSE UNDER 37 C.F.R. § 1.116

Commissioner for Patents
U.S. Patent and Trademark Office
Customer Service Window, Mail Stop Amendment
Randolph Building
401 Dulany Street
Alexandria VA 22314

Sir:

In response to the Final Official Action of May 1, 2009, in which a three-month shortened statutory period for response was set to expire on August 3, 2009 (August 1 being a Saturday), Applicants respectfully request reconsideration and withdrawal of the outstanding rejections set forth in the above-mentioned Final Official Action in view of the herein contained amendments and remarks.

AMENDMENTS TO THE CLAIMS

The claims in this listing will replace all prior versions, and listings, of claims in the application.

LISTING OF CLAIMS

1. (Currently Amended) An electronic component mounting method in which joints between a circuit substrate and electronic components are reinforced using a resin, the method comprising:

supplying an unhardened reinforcing resin on the circuit substrate;

~~supplying~~ printing a solder paste on the reinforcing resin such that the reinforcing resin is disposed between the solder paste and bond areas of the circuit substrate;

placing the electronic components, which have solder bumps, on the circuit substrate; and

heating the reinforcing resin, the solder bumps and the solder paste,

wherein the solder paste flows through the reinforcing resin and contacts the bond areas of the circuit substrate to interconnect the circuit substrate and the electronic components in response to heating of the reinforcing resin.

2. (Previously Presented) The electronic component mounting method according to claim 1,

wherein the reinforcing resin is a sheet-form resin, and the method further comprises cooling the reinforcing resin and the solder paste, thereby solder-bonding the electronic components on the circuit substrate and hardening the resin.

3. (Currently Amended) The electronic component mounting method according to claim 2, wherein the sheet-form resin includes equally spaced apertures forming a matrix of pores.

4. (Previously Presented) The electronic component mounting method according to claim 2, wherein the sheet-form resin includes recesses at positions that match electrode bond areas on the circuit substrate.

5. (Previously Presented) The electronic component mounting method according to claim 2, wherein the sheet-form resin includes holes at positions that match electrode bond areas on the circuit substrate.

6. (Currently Amended) An electronic component mounting method in which joints between a circuit substrate and electronic components are reinforced using a resin, the method comprising:

printing a solder paste on bond areas of the circuit substrate where electrodes of the electronic components are to be bonded; then

restricting fluidity of the solder paste so that the solder paste retains its shape as printed; then

applying a thermosettable reinforcing resin on the circuit substrate including the solder paste; then

placing the electronic components, which have solder bumps, on the circuit substrate; and then

solder-bonding the electronic components on the circuit substrate and hardening the reinforcing resin.

7. (Previously Presented) The electronic component mounting method according to claim 6, while restricting fluidity of the solder paste, the fluidity is controlled such that the solder paste retains its shape as printed during the application of the reinforcing resin but deforms when a load is applied when the electronic components are mounted.

8. (Previously Presented) The electronic component mounting method according to claim 7, while restricting the fluidity of the solder paste, the solder paste is dried so as to volatilize the solvent or the like in the solder paste.

9. (Previously Presented) The electronic component mounting method according to claim 8, wherein the solder paste covering a substantially entire area on the circuit substrate or covering a specified area is selectively dried.

10. (Previously Presented) The electronic component mounting method according to claim 8, wherein drying is carried out using any of hot air, a heater, microwave, and light or using vacuum drying method.

11. (Previously Presented) The electronic component mounting method according to claim 6, wherein the reinforcing resin is applied on a substantially entire area of the circuit substrate or on a specified area selectively.

12. (Previously Presented) The electronic component mounting method according to claim 6, wherein the reinforcing resin is a resin material having a flux effect.

13. (Previously Presented) The electronic component mounting method according to claim 6, wherein the reinforcing resin is used that has an effect of bonding the electronic components to the circuit substrate.

14. (Previously Presented) The electronic component mounting method according to claim 6, wherein the mounted electronic components are retained by deformation of the solder paste that deforms by a mounting load and by adhesive power of the reinforcing resin.

15-19. (Cancelled)

REMARKS

Claims 1-14 remain pending in the application. Claims 1, 3 and 6 are amended. Reconsideration of the rejection and allowance of the pending application in view of the following remarks are respectfully requested.

In the Office Action, the Examiner rejected claim 1 under 35 U.S.C. §102(b) as being anticipated by Zhou et al. (U.S. Patent No. 5,985,043).

Applicants' claim 1, as currently amended, recites an electronic component mounting method in which joints between a circuit substrate and electronic components are reinforced using a resin. The method includes supplying an unhardened reinforcing resin on the circuit substrate, printing a solder paste on the reinforcing resin such that the reinforcing resin is disposed between the solder paste and bond areas of the circuit substrate, placing the electronic components, which have solder bumps, on the circuit substrate, and heating the reinforcing resin, the solder bumps and the solder paste. The solder paste flows through the reinforcing resin and contacts the bond areas of the circuit substrate to interconnect the circuit substrate and the electronic components in response to heating of the reinforcing resin.

Zhou et al. discloses a method of attaching a substrate to a device. In this method, a flux composition 120 is coated on a surface of a substrate 100, solder bumps 140 are provided on a flip chip 130, and a metallization pattern 110 is provided on the substrate 100. See, e.g., Fig. 1 and col. 10, lines 3-9 of Zhou et al. The chip 130/230 is moved into contact with the metallization pattern 110/210, and an assembly 270 of these elements is reflowed in an oven. See, e.g., Fig. 2 and col. 10, lines 10-23 of Zhou et al. Zhou et al. also discloses that instead of the solder bumps 140, a solder paste comprising a solder powder and the composition 120 can be employed. See col. 10, lines 40-43 of Zhou et al.

Applicants respectfully submit that Zhou's method does not include printing a solder paste on a reinforcing resin. Rather, Applicants submit that Zhou's solder paste is a mixture of the flux composition 120 and a solder powder. See, e.g., col. 10, lines 40-43 of Zhou et al. Thus, Zhou's solder paste is not printed on the flux composition 120.

Applicants further submit that Zhou's method does not utilize both a solder paste and solder bumps which are formed on electronic components. In contrast, Zhou et al. discloses that solder paste may be employed instead of the solder bumps 140. See, e.g., col. 10, lines 40-43 of Zhou et al.

Thus, Applicants respectfully submit that Zhou et al. does not disclose an electronic component mounting method which includes supplying an unhardened reinforcing resin on a circuit substrate, printing a solder paste on the reinforcing resin such that the reinforcing resin is disposed between the solder paste and bond areas of the circuit substrate, placing electronic components, which have solder bumps, on the circuit substrate, and heating the reinforcing resin, the solder bumps and the solder paste, as recited in Applicants' amended claim 1.

For at least these reasons, Applicants submit that Zhou et al. does not anticipate the invention recited in Applicants' claim1, and requests that the Examiner withdraw the rejection under 35 U.S.C. §102(b).

In the Office Action, the Examiner rejected claims 2-5 under 35 U.S.C. §103(a) as being unpatentable over Zhou et al. in view of Nakamura et al. (U.S. Patent No. 6,365,499). Applicants respectfully submit that Nakamura et al. does not overcome the above-noted deficiencies of Zhou et al. with respect to claim 1, and thus requests that the Examiner withdraw the rejections of claims 2-5, in view of their dependency from claim 1.

In the Office Action, the Examiner rejected claims 6-14 under 35 U.S.C. §103(a) as being

obvious over Zhou et al. (U.S. Patent No. 5,985,043) in view of Hayama et al. (U.S. Patent No. 6,051,448).

Applicants' claim 6, as currently amended recites an electronic component mounting method in which joints between a circuit substrate and electronic components are reinforced using a resin. The method includes, inter alia, printing a solder paste on bond areas of the circuit substrate, then restricting fluidity of the solder paste, then applying a thermosettable reinforcing resin on the circuit substrate, then placing the electronic components, which have solder bumps, on the circuit substrate, and then solder-bonding the electronic components on the circuit substrate and hardening the reinforcing resin.

In the Final Office Action, the Examiner acknowledges that Zhou et al. does not disclose that the flux composition is printed on the substrate 100. However, the Examiner asserts that it would have been obvious to print Zhou's flux composition 120 on the substrate 100, citing Hayama et al. Applicants respectfully disagree.

Zhou et al. discloses that the flux composition 220 wets a flip chip 230, insuring complete coverage of an active surface 250 of the chip 230. See, e.g., Fig. 2 and col. 10, lines 10-14 of Zhou et al. During reflow and hardening, the flux composition 220 encapsulates the chip assembly 270. See, e.g., col. 10, lines 31-35 of Zhou et al.

Applicants respectfully submit that if Zhou's flux composition 120/220 were to be printed on the substrate 100/200, as the Examiner suggests, the flux composition 120/220 would not completely cover the active surface 250, and the assembly would not be encapsulated by the flux composition 120/220. For at least these reasons, Applicants submit that it would not have been obvious to print Zhou's flux composition on the substrate.

Further, in the Final Office Action, the Examiner asserts that the fluidity of Zhou's flux composition is restricted. In the method of Applicants' claim 6, a thermosettable reinforcing resin is applied after a solder paste is printed, and after fluidity of the solder paste is restricted. The Examiner appears to be taking the position that applying the flux composition 120 to the substrate 100 reads on both the "printing" and "applying" steps of Applicants' claim 6. As discussed above, Zhou et al. discloses that the solder paste is a mixture of the flux composition 120 and a solder powder. However, Zhou et al. does not suggest a method which includes both printing a solder paste and applying a thermosettable reinforcing resin, and does not suggest applying a thermosettable reinforcing resin after the fluidity of the flux composition is restricted, as recited in Applicants' claim 6.

Further, in the method of Applicants' claim 6, the electronic components are placed on the circuit substrate after the fluidity of the solder paste is restricted. In contrast, Zhou et al. discloses that the chip 130/230 is placed on the substrate 100/200 before reflow and hardening of the flux composition 120/220 is performed. See, e.g., col. 10, lines 10-35 of Zhou et al.

Further, as discussed above, Zhou's method does not utilize both a solder paste and solder bumps which are formed on electronic components. In contrast, Zhou et al. discloses that solder paste may be employed instead of the solder bumps 140. See, e.g., col. 10, lines 40-43 of Zhou et al.

In view of the above, Applicants respectfully submit that the combined teachings of Zhou et al. and Hayama et al. do not disclose or suggest an electronic component mounting method which includes printing a solder paste on bond areas of a circuit substrate, then restricting fluidity of the solder paste, then applying a thermosettable reinforcing resin on the circuit substrate, then placing electronic components, which have solder bumps, on the circuit substrate,

and then solder-bonding the electronic components on the circuit substrate and hardening the reinforcing resin, as recited in Applicants' amended claim 6.

Accordingly, Applicants respectfully request that the Examiner withdraw the rejections of claims 6-14 under 35 U.S.C. §103(a).

Based on the above, it is respectfully submitted that this application is in condition for allowance, and a Notice of Allowance is respectfully requested.

SUMMARY AND CONCLUSION

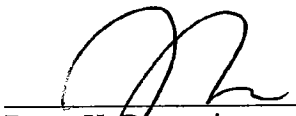
Reconsideration of the outstanding Office Action, and allowance of the present application and all of the claims therein are respectfully requested and believed to be appropriate. Applicants have made a sincere effort to place the present invention in condition for allowance and believe that they have done so.

Any amendments to the claims which have been made in this amendment, and which have not been specifically noted to overcome a rejection based upon the prior art, should be considered to have been made for a purpose unrelated to patentability, and no estoppel should be deemed to attach thereto.

Should an extension of time be necessary to maintain the pendency of this application, including any extensions of time required to place the application in condition for allowance by an Examiner's Amendment, the Commissioner is hereby authorized to charge any additional fee to Deposit Account No. 19-0089.

Should the Examiner have any questions or comments regarding this response, or the present application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
Masato MORI et al.



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